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# A HIGHLY RECONFIGURABLE FFT ARCHITECTURE FOR 3G/4G TECHNOLOGIES

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Abstract - A low-power dynamic reconfigurable FFT is proposed for accurate spectral analysis. The architecture is served as a scalable IP Core which is suitable for System on Chip applications. The system can be configured as 64, 128, 256, 512, 1024 and 2048-point FFT by using multiple processor on chip. Compared with a conventional ASIC FFT processor, this reconfigurable FFT design is characterized by having dynamic reconfigurability. Pipelined architecture for testing is proposed to achieve complexity reduction of NOC. Compared with a FFT processor which is mapped onto a general purpose reconfigurable architecture, it has 30~94% less energy consumption.

## I. INTRODUCTION

Accurate frequency estimation of distorted and noisy signals in industrial power systems is a challenging problem that has attracted much attention. In power systems, the typical application of frequency estimation is for protection against loss of synchronism, under-frequency relaying, power-quality monitoring, and power system stabilization. De-noising and frequency recognition are of critical importance in practical deployment of signal communications. Many de-noising techniques exist in the literature. However, few of them are based on a general and rigorous framework, while at the same time demonstrating effectiveness in large-scale robust multi tone frequency recognition experiments. A key point of this work is to use of a strong on chip testing recognition model. The proposed built in self testing algorithm incorporates prior knowledge about the structure of signals, noise model, which is essential to its performance. A new method for frequency estimation technique is proposed using on chip built in self testing. In any case, the accuracy of the frequency estimation provided by the FFT is affected by errors due to the wideband noise superimposed onto the acquired data in the practical applications. There is a necessity to investigate the statistical behavior of the frequency estimation of distorted and noisy harmonic signals provided by simple and accurate interpolation algorithm. The reasons are given here. 1) The influence of a stationary white noise on the frequency estimation provided by the multipoint interpolation FFT based on the maximum side lobe decay window has been analyzed. The frequency estimations are based on the FFT which uses the direct ratio of two maximum amplitude spectral lines and thus contains even items. However, there is a lack of the expression of the statistical behavior of the frequency estimation by the non-even item interpolation algorithm, which can avoid the even items in the spectral-peaks polynomial fitting procedures and provide fast and very high accuracy frequency estimation. 2) It is well known that spectral leakage suppression is obtained at the cost of widening the main lobe, and this increases noise contributions. In scientific literature, the accuracy of frequency estimation has been derived only for the FFT with the cosine windows. Since the self-convolution windows own good sidelobe behaviors, it is important to know the influence of self-convolution windows on the accuracy of frequency estimation.Digitally assisted analog design and integrated transceiver calibration approaches are gaining popularity in ensuring efficient and reliable mixed-signal systems in nano scale CMOS technologies. One design aspect is to equip analog blocks with performance-tuning features that allow the recovery from process variations and faults. Examples of such tuning mechanisms include input impedance matching, gain and center frequency tuning for low-noise amplifiers, second-order nonlinearity and mismatch correction for mixers, as well as linearity enhancements for baseband filters. The other aspect related to digitally assisted design is the extraction of performance metrics on the chip to enable one-time or periodic calibrations. Many performance characteristics can be observed based on the output spectrum of a circuit under test (CUT) or a chain of analog blocks, which has led to on-chip spectrum analyzers that emulate conventional off-chip instrumentation. Alternatively, calibration methods have been proposed that incorporate existing or dedicated analog-to-digital converter (ADC) and digital signal processing resources to directly quantize the output signals of analog circuits for the computation of the fast Fourier transform (FFT) and automatic tuning with digital-to-analog converters (DACs). Extraction of circuit linearity parameters with the latter approach calls for efficient FFT implementations, which is the focus of this paper.

The presented method leverages that the frequencies for two-tone tests can be selected by the designer of the built-in test (BIT) or built-in calibration (BIC) scheme to circumvent inaccuracies due to spectral leakage while using a small number of FFT points. This capability to accurately measure the power of the tones as well as their distortion and inter modulation products with an efficient on-chip FFT can also find application in loopback testing techniques with spectral estimation.

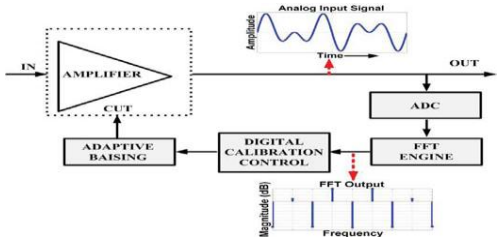



Fig 1.On-chip BIC approach with spectral testing

## II.RELATED WORK

The on-chip spectrum analyzeruses a digital frequency synthesizer [1]and a simple signal generator synchronized with a switched capacitor band pass filter. It consists of a digital frequency synthesizer, a switched-capacitor (SC) sine wave generator, a SC Band pass filter, a variable gain amplifier (VGA) and a final stage for the amplitude detection and/or digitization of the VGA output.pipelined FFT architecture, called mixed-radix multipath delay feedback (MRMDF), can provide a higher throughput rate by using the multi data-path scheme[2]. Furthermore, the hardware costs of memory and complex multipliers in MRMDF are only 38.9% and 44.8% of those in the known FFT processor by means of the delay feedback and the data scheduling approaches. The high-radix FFT algorithm is also realized in our processor to reduce the number of complex multiplicationsThe cosine-class windows are some of the most used windows in analog to digital converter (ADC) dynamic testing [3] by spectral analysis when the coherent sampling condition cannot be fulfilled. A new indexed-scaling method is proposed to reduce both the critical-path delay[4] and hardware cost by employing shorter word length. Together with the mixed-radix multipath delay feedback structure, the proposed FFT processor can achieve very high throughput with low hardware cost. We explore the reuse of built-in digital calibration circuitry, along with minor digital design-for-testability (DfT)[5] modifications, to test and characterize analog/RF circuit performance. By observing the digital tuning signals captured in the digital calibration circuitry, the analog/RF performance can be closely estimated, thus enabling cost-effective Go/No-Go production testing. The realization of an on-chip block for built-in testing of RF transceivers[6] with the loopback method.The circuit is intended for cost-efficient production testing of RF front-end blocks with on-chip power detectors. A traditional loopback scheme is re-configured with an analog filter and an adder implemented on a Device Interface Board (DIB), and a multiple tone input is applied to the DUTs.The spectral predictors are obtained from the Fourier representation of the loopback response[7] by measuring the magnitude of its fundamentals and harmonics.

## III. PROPOSED APPROACH

Generally FFT is used for time to frequency transform at receiver end in wireless communication (e.g. 3G & 4G). Since all processing units are designed inside chip, there is possibility get distortion in spectrum due to single tone frequency or multi tone frequency or due to chip malfunctions. To get accurate spectrum or signal, we have to find out error or losses in spectrum. A built in spectrum analysis and calibration approach is proposed. This design analyzes spectrum samples of FFT output to determine distortions. Then Calibration tunes spectrum into required level. However this paper proposed FFT for 16 points that cannot be applicable for $4^{th}$ generation technologies. Also it has fixed sampling rate method failed to maintain tradeoff between speed and resolution. Here we propose a reconfigurable architecture that supports multiple inputs FFT for future communication technologies with tradeoff between speed and accuracy using reconfigurable pulse width modulation.

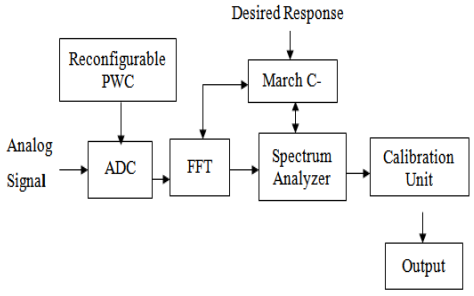



Fig 3.1 Block Diagram

*a) ADC*

It is a device that converts continuous physical quantity to digital number. Conversion involves Quantization of input, so it introduces small amount of error. Instead of doing a single conversion, ADC performs conversion ('Samples' the input) periodically. ADC is defined by its Bandwidth (the range of frequency it can measure) and it's SNR (how accurately it can measure a signal relative to the noise it introduces).

*b) Sample and Hold*

It is to sample an analog input signal and hold this value over a certain length of time until the ADC can process the information.A/D Conversion involves a two step process:

1. Quantizing is breaking down the analog value into a set of finite states.
2. Coding is assigning digital word or number to each state

*c) SAR Architecture*

Successive approximation employs a binary search algorithm in a feedback loop including a 1 bit A/D converter. The Following Figure 3.3: illustrates architecture which consists of a front end track & hold circuit, comparator, DAC and SAR logic. SAR logic is basically a shift register combined with decision logic and decision register. The pointer points to the last bit changed in the decision register and the data stored in this register is the result of all comparisons performed during conversion period

*d) Track & Hold*

A sample-and-hold (S/H) or track-and-hold (T/H) circuit is frequently required to capture rapidly varying signals for subsequent processing by slower circuitry. The function of the S/H circuit is to track/sample the analog input signal and to hold that value while subsequent circuitry digitizes it. The function of a track-and-hold circuit is to buffer its input signal accurately during track mode providing at its output a signal which is linearly proportional to the input, and to maintain a constant output level during hold mode equal to the T/H output value at the instant it was strobe from track to hold by an external clock signal.

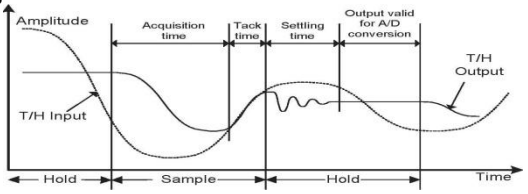
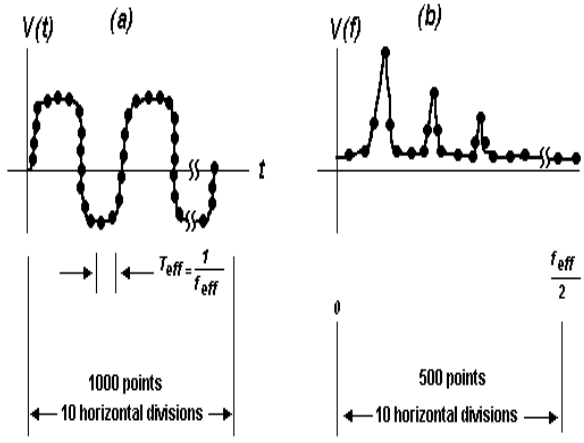



Figure 3.2 waveforms of a practical sample-and-hold circuit.

*I. FAST FOURIER TRANSFORM*

a) Testing with the Fast Fourier Transform

The simplest frequency-domain tests use the direct application of the fast Fourier transform. Taking the FFT of the output data while driving the A/D converter with a single, low distortion sine wave, the SNDR, ENOB, SFDR, and THD can easily be calculated. It is useful to take these measurements at several input amplitudes and frequencies, and plot the results. Taking data for high input frequencies allows the full-power and full-linear bandwidths to be calculated.Two more tests are completed while driving the A/D converter with an input composed of two sine waves of different frequencies. The FFT of this test result is used to calculate the IMD (for second-order and third-order products) and the two-tone SFDR.The discrete (or digitized) version of the Fourier transform is called the Discrete Fourier Transform (DFT). This transform takes digitized time domain data and computes the frequency domain representation. While normal Fourier theory is useful for understanding how the time and frequency domain relate, the DFT allows us to compute the frequency domain representation of real-world time domain signals. This brings the power of Fourier theory out of the world of mathematical analysis and into the realm of practical measurements. The Agilent 54600 scope with Measurement/Storage Module uses a particular algorithm, called the Fast Fourier Transform (FFT), for computing the DFT. The FFT and DFT produce the same result and the feature is commonly referred to as simply the FFT.




*II. FFT Implementation*

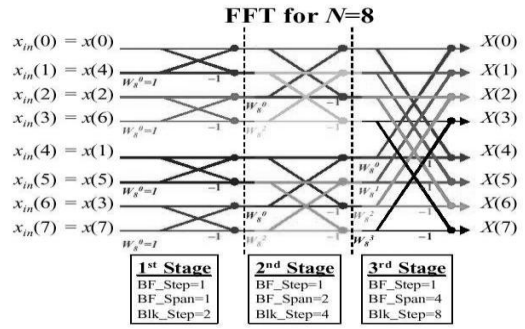



Fig 3.3 FFT implementation

we can see the different stages. In stage 1, there are 4 blocks, with one butterfly-per-block. In stage 2, there are two blocks with 2 butterflies each; and finally, in stage 3, there is only one block, combining all 8 coefficients with 4 butterflies.

*Decimation in time FFT:*

Number of stages = $\log_2 N$

Number of blocks/stage = $N/2^{stage}$

Number of butterflies/block = $2^{stage-1}$

Table 1
FFT Implementation

| | | | |
|---|---|---|---|
| Start Index | 0 | 0 | 0 |
| Input Index | 1 | 2 | 4 |
| Twiddle Factor Index | N/2=4 | 4/2=2 | 2/2=1 |
| Indices used | W0 | W0 | W0 |
| | | W2 | W1 |
| | | | W2 |
| | | | W3 |

## III. Layout Design

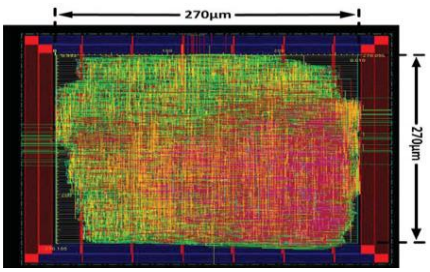



Fig 3.4 Layout of the FFT engine (0.73 mm2 in 45-nm CMOS technology)

## IV. SIMULATION AND OUTPUT

*A) Output forfixed point FFT verification*

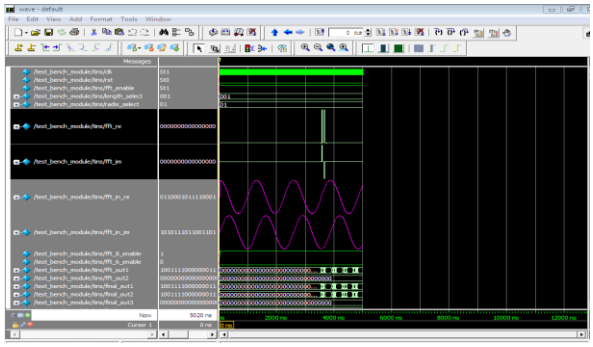


Fig.4.1 Fixed point FFT verification with sine & cosine waves

*B) Output for sample selection*

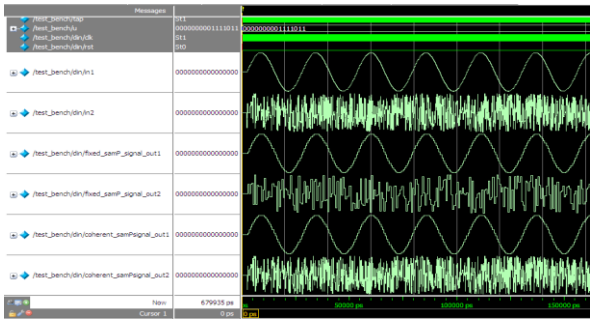


Fig.4.2 sample selection with fixed rate for single and multi tone signals

C) *FFT spectrum for multi tone signals with variable point FFT*

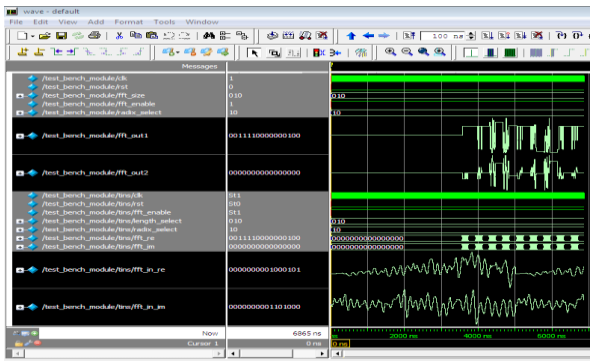


Fig 4.3 spectrum for multi tone signals with variable point fft

*D) Spectrum for multi tone signals using coherent sampled*

*FFT*

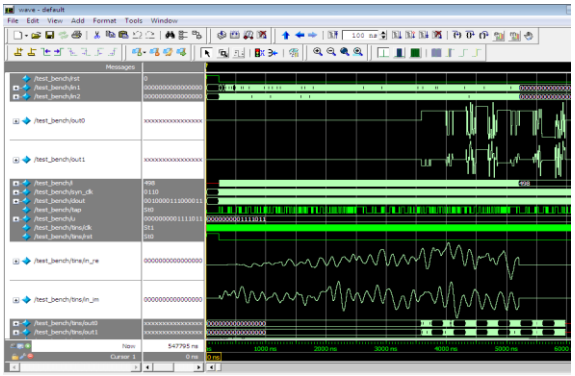


Fig.4.4 FFT spectrum for multi tone signals with fixed point coherent sampled FFT

*E) Area optimization*

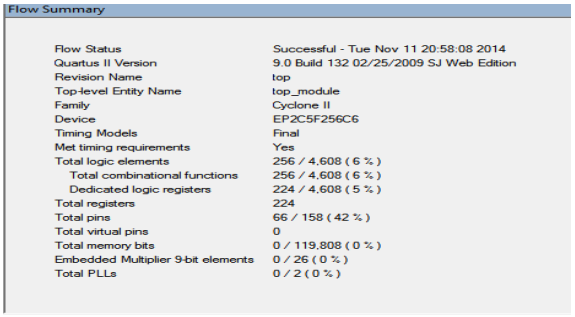



TABLE II

Comparison for fixed point and variable point FFT

| FFT type | Area complexity | Speed | Power |
|---|---|---|---|
| Fixed point FFT | 256 | 4.079 Ps | 46.37 mw |
| Variable point FFT | 1025 | 5.952 Ps | 68.09 mw |

## VI. Conclusion

Here , we proved that coherent sampling based FFT will give better hardware complexity & power optimization with considerable delay enhancement. An accurate FFT-based analysis approach was introduced for FFT core with single and multi tone point spectral characterizations. The proposed approach was derived from the coherent sampling method. The method avoids the use of a large number of FFT points to minimize the required FFT resources for area- and power-efficient built-in testing applications. Modelsim based pre simulation results of an FFT implementation showed the feasibility of the approach. For a QUARTUS II based hardware synthesis report of 16-point FFT computation, the implemented FFT engine consumes an estimated power of 46.37mW and occupies an area of 256 LE's which almost 4 times less as compared to variable point FFT.

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