ISSN 23499842(Online), Volume 1, Special Issue 2(ICITET 15), March 2015
International Journal of Innovative Trends and Emerging Technologies

A New VLSI Architecture of Efficient Radix based Modified Booth Multiplier with Reduced Complexity

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***Abstract*—The Multiply-Accumulate Unit (MAC) is the main computational kernel in DIP architectures. The MAC unit determines the power and the speed of the overall system; it always lies in the critical path. Developing high speed and low power MAC is crucial to use DSP in the future WSN. In this work, a fast and low power signed MAC Unit is proposed with reconfigurable Modified booth algorithm (MBE). The proposed architecture is based on modified booth radix-8 with merged MAC architectures to design a unit with a low critical path delay and low hardware complexity. Here booth based approach for partial products generations and Tree based approach for partial products reduction in multiplications .The new architecture reduces the hardware complexity of the summation network using tree based carry select adder (CSA) & carry look ahead (CLA) , thus reduces the overall power and complexity. Increasing the speed of operation is achieved by feeding the bits of the accumulated operand into the summation tree before the final adder instead of going through the entire summation network. The FPGA implementation of the proposed signed booth radix-8 based MAC unit can save considerable amount of the area with significant performance enhancement as compared to the regular merged MAC unit with conventional multiplier.**

Keywords: ***Digital Signal Processing (*DSP*), Multipy & Accumulate (MAC), Radix-8 MB (Modified Booth). Very Large Scale Integration (VLSI).***

I. INTRODUCTION

The applications of the digital images are more and more extensive today than ever before. In recent years, the design for high speed with low power consumption has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to reduce the power consumption with high performance of new VLSI systems. However, most of these methods focus on the power consumption and quality enhancement by replacing multipliers with distribute arithmetic approach [1]-[2]. But this increase the overall delay makes them unsuitable for high speed applications. software implementation, but unfortunately due to their irregular structure and complex routing, these algorithms are not suitable for VLSI implementation. Our goal is to design a high speed signed MAC suitable for FIR filters. To reduce the area of the MAC circuit, moderate partial product reduction methods are most widely used but it will lead propagation delay, many compensation methods like parallel computations are used in many cases to solve this problem [3]-[4].
Here we attempt to increase the speed of multiplication by reducing number of partial products generated using efficient radix-8 modified booth table. The main concerns are speed and hardware complexity in MAC computation and its signed counterpart for image processing application intent.

II. FPGA IMPLEMENTATION

Field programmable gate arrays were actually invented only for prototyping the digital design which is later to be used in IC's. But in recent days FPGA's are started to use as a product in many fields. So Field programmable gate arrays are ideally suited for the implementation of DCT based digital image compression. However, there are several issues that need to be solved. When performing software simulation of DCT, calculations are carried out with signed arithmetic. But in FPGA design measures to be taken to account for this. Another concern is the DCT computation itself. Both for forward transform and it inverse multipliers with variable sizes are required. Many techniques [5]-[8] have been used to efficiently cover these features in MAC for digital implementation.

Multiplier unit is always being the key component to achieve a high performance digital system.

Two ways to achieve efficiency in MAC are

1. To reduce the number of partial products to be added by encoding, one of the input operands. Modified Booth algorithm [10] is one of the most popular approaches.

2. Hardware will be reused [8] for partial products addition that determines the performance of the multiplier

Here we combine both method 1 & 2 for MAC for computation.

III. BOOTH MULTIPLIER

In the modern world, we need system which will run at high speed. Multipliers play an important part in today's DSP and DIP applications. In our case for DCT computation multiplications are used larger in number. Therefore, speed improvement in multiplier is important. Advances in technology have permitted many researchers to design multipliers which offer both high-speed and unique hardware structure, thereby making them suitable for specific VLSI implementation.

In any multiplication algorithm, the multiplication operation is carried out by summation of decomposed partial products. For high-speed multiplication we need to apply a booth radix recoding multiplication algorithm. In recent days in all high radix booth algorithm recoding is changed from 2s-complement format to a signed-digit representation from the defined set. This is called modified booth algorithm..

A. Radix-8 Algorithm

Here we reduce the number of partial products using a higher radix in the multiplier recoding. Recoding of binary numbers was first invented by Booth [5]. The modified Booth's algorithm is done by appending a zero to the right of M. Figure 1 shows recoding of $01010101_{2.}$ In radix-8 recoding is similar to radix-4 [6] but here we take four bits instead of three bits and then we represent that coded values in signed-digit representation using TABLE I.

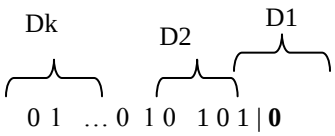

Fig 1: Recoding representation

Where *k* is the number of partial products to be generated.

TABLE I. Radix-8 sign digit values

Coded bits	signed-digit value
0000	0
0001	+1
0010	+1
0011	+2
0100	+2
0101	+3
0110	+3
0111	+4
1000	-4
1001	-3
1010	-3
1011	-2
1100	-2
1101	-1
1110	-1
1111	0

From the TABLE I we need to have 2N, 3N, 4N and its 2's complement respectively.

B. Preprocessing Stage.

Both 2N and 4N is achieved by simple left shift of N. and 3N is calculated by adding 2N and N. If the bit width of N is high this will increase the delay in preprocessing stage. After this stage only we can generate partial products. In order to reduce the delay here we use Carry select adder. The resource used in CSA adder later will be used for partial product addition.

C. TREE BASED PP REDUCTION

Truncation errors will occur when we remove least significant bits from multiplied result. Here we use Wallace array to represent partial products array and its summation, which gives the multiplication result. First four partial products are processed using 4-

2 compressor which is made up of two full adders. In later stages we used only Full adder for partial product addition.

Normally, multiplication involves two basic operations as partial production generation and their partial product summation. The main bottle-neck of the area is in the multiplication of two numbers as it generates a product with twice the original bit width.. The critical path for the multiplier is on the number of partial products. The partial products generated are added using Wallace Tree Compressor (WTC).The basic idea of this work is to use WTC instead of CPA to achieve lower area and power consumption. The main advantage of this WTC logic reduces the number of full adders and half adders during the tree reduction. The design achieves less area and power.

In radix-8 partial products are left shifted by three bits. So in partial products some of the LSB bits will become 0's. It is predefined one. So these bits are not considered here in Wallace tree structure in order to save the hardware resource. In Wallace tree partial products are divided into main part and truncation part. Resource used in truncation part is reconfigured based on number of columns need to be selected for error compensation.

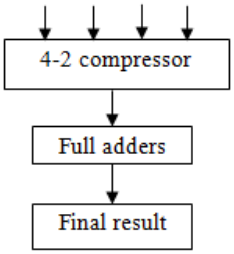

Fig 2**:** Wallace tree structure

D. FIR FILTER

Filtering is an operation usually performed to extract the needed information from a digital signal.

FIR Filter consists of 2 things:

1. A Sample delay line
2. Set of coefficients.

In a single-rate filter, the output result rate is equal to the input sample rate. The filter output y(k) is computed according to following equation. where *N* is the number of filter coefficients *a(n) n = 0….N - 1* are the filter coefficients and *x(n)* represents the input samples.

$$y(k) = \sum_{n=0}^{N-1} a(n)x(k-n)$$

E. PROPOSED SYSTEM

In this work, a fast and low power MAC Unit is proposed for 2D-DCT computation. Multiplication involves the generation of partial products, one for each digit in the multiplier, These PP are then summed to produce the final product.

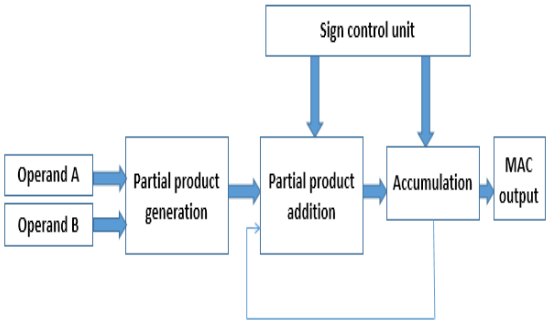

Fig 4.3 Proposed MAC unit

IV. PERFORMANCE ANALYSIS

The design is scripted as a verilog HDL file and synthesized using QUARTUS II 9.0 v. The design is synthesized into Cyclone device. Performance metric of tree based methodologies over conventional partial precuts addition is proved in terms speed and area efficiency. Higher order booth will always leads better throughput but cares to be taken to keep the reconfigurability.

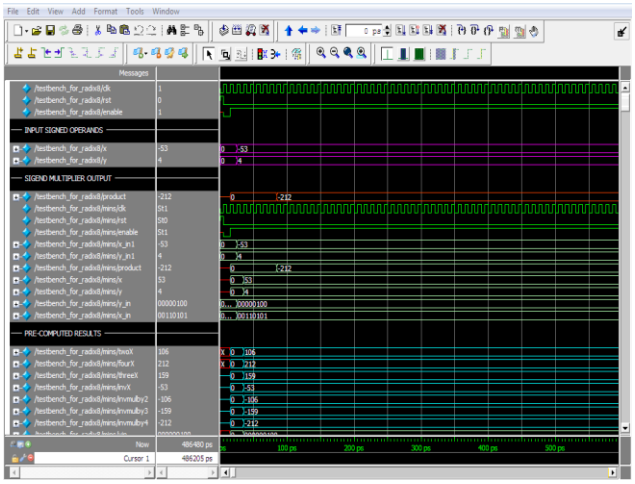

Fig 3: Simulated Output

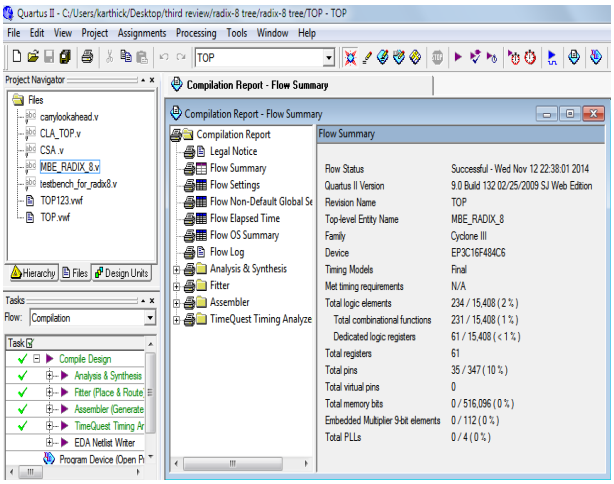

Fig 4: Area Utilization Summary

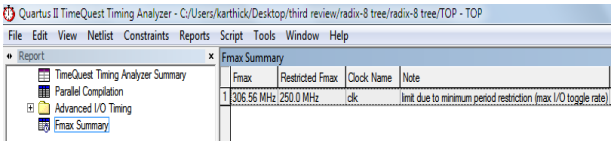

Fig 5: Operating Frequency Report

TABLE II
COMPARISON OF PARAMETRS

TYPE	AREA(LE's used)	SPEED
Conventional(array type)	327	129.57 MHz
Booth radix-4	285	239.35 MHz
Booth radix-4 tree based	264	265.89 MHz
Booth radix-8 tree based	234	306.56 MHz

V. CONCLUSION

In this paper, a unique high speed booth multiplier based MAC unit is implemented to increase throughput rate. It has been proved the adoption of the proposed recoding technique delivers optimized solutions for the general MAC unit. By using the Carry select level adder and Carry Look Ahead Adder, achieved the optimized results in both area and speed. As this type of multiplier are used in DSP applications like FFT, Digital Image processing because it performs both signed and unsigned multiplication. It has been proved that it can be useful to apply radix-8 architecture in high-speed multipliers for application specific designs. The results verify that the proposed architecture has high performance and requires less hardware complexity than traditional implementation digital MAC units on FPGA.

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